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14. ABSTRACT

High current density field emission (FE) cathodes were studied as a long sought alternative to thermionic cathodes which must operate above 1100°C in order to meet the performance required for the HiFive program. A back-gate design with the gate electrode positioned behind the array of FE tips was studied as a way to minimize the chance of arching. The use of diamond as the emitter material provided a robust, low effective work function material coupled with a tip radius of ~ 5nm to provide high field enhancement. Modeling predicted field enhancement as a

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Report Title

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List of papers submitted or published that acknowledge ARO support during this reporting period. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

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Graduate Students

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Names of Post Doctorates

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Names of Faculty Supported

NAME	PERCENT_SUPPORTED	National Academy Member
Weng Poo Kang	0.30	No
Jim Davidson	0.30	No
FTE Equivalent:	**0.60**	
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Names of Under Graduate students supported

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period:	0.00
The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields:.....	0.00
The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields:.....	0.00
Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):	0.00
Number of graduating undergraduates funded by a DoD funded Center of Excellence grant for Education, Research and Engineering:	0.00
The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense	0.00
The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields:	0.00

Names of Personnel receiving masters degrees

NAME
Total Number:

Names of personnel receiving PHDs

NAME
Total Number:

Names of other research staff

NAME	PERCENT SUPPORTED	
Gary McGuire	0.02	No
Olga Shenderova	0.17	No
William Mecouch	0.24	No
Brian Schultz	0.01	No
Garry Cunningham	0.01	No
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Back-gated Diamond Field Tip Array Cathodes for 220 GHz TWT

Contract #W911NF-08-C-0052

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December 29, 2009

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Section I Summary of the Report

High current density field emission (FE) cathodes are a long sought alternative to thermionic cathodes which must operate above 1100 °C in order to meet the performance required for the HiFive program. The so-called “cold cathodes” operate on the principle of potential barrier lowering and tunneling of electrons into the vacuum at high electric fields. Due to catastrophic arching leading to failure of the entire device and the inability to achieve the projected currents as a result of scaling of small area arrays to large ones, previous FE cathode designs have not yet been implemented in fielded applications. The back-gate design with the gate electrode positioned behind the array of FE tips minimizes the chance of arching. Further, the close proximity of the gate electrode to the emitter tips separated only by a thin intervening dielectric allows low gate voltage operation, <125 V, and as a consequence the energy of ions produced in the vicinity of the cathode is low and less likely to cause damage. The use of diamond as the emitter material provides a robust, low effective work function material that can be grown in silicon molds with a tip radius of ~ 5nm providing high field enhancement. Dopants introduced during chemical vapor deposition of diamond provide the electrically conductive tips and a separate more resistive barrister layer, which serves as a means to achieve more uniform electron emission across an array.

Modeling provided an optimum layout for the pitch between the diamond tips along the cathode lines as well as the pitch between cathodes lines. The field enhancement as a result of voltage applied to the back-gate was predicted to be between 10^2- 10^3 which is consistent with the previous experimental result of ~250. Diamond tip arrays laid out in the geometry suitable for the HiFive program have been fabricated and tested. A total emission current of 600 mA at 6.1A/cm^2 was produced matching the best know reported current from a single cathode. The best current density, 15 A/cm^2, at a high emission current 15 mA is among the highest reported for FE cathodes in light of achieving simultaneously both high current and current density. Both sets of data were obtained in pulse mode. The modeling predicts that the HiFive program goal of 750 A/cm^2 can be met with the present design and scaling the tip base as a next step to increase the tip density and enhance the electrostatic field at the tip will more than double the current and current density providing cathodes that exceed the requirements of the HiFive program without additional

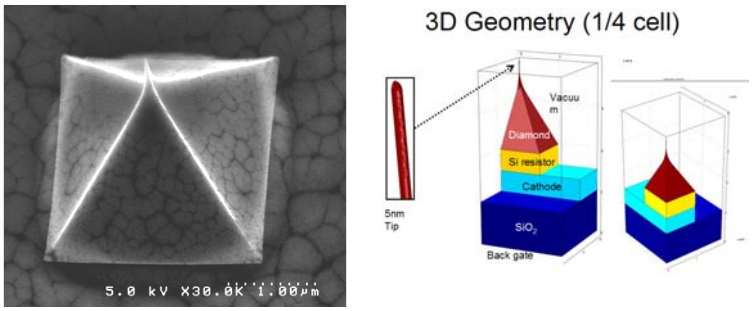


Fig.1 Electrostatic simulation of back-gate cathodes with diamond tip (right) arrays predicts current modulation of between 10^2-10^3 to achieve program goal of 750 A/cm^2.

enhancements.

Process studies were conducted to achieve predictable yield of diamond tips with small radius. A barrister layer was developed as a base layer for the diamond tip array as a means to achieve more uniform electron emission across an array of tips. A process was developed to integrate the back-gate electrode with the diamond tip array taking into consideration a variety of issues such as the deposition process, adhesion, etch selectivity, and coefficient of thermal expansion. The process is poised upon review to produce cathodes for the HiFive program and other applications.

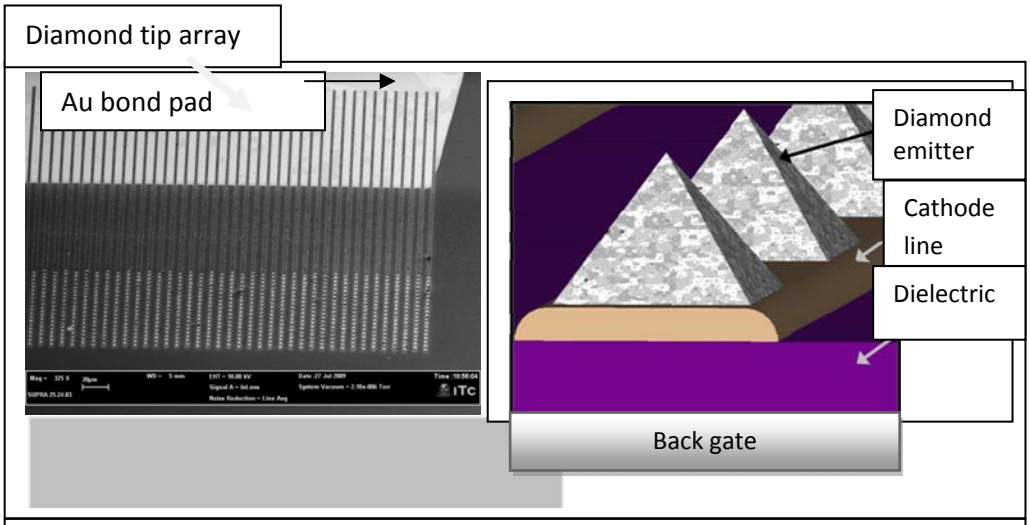


Fig. 2 SEM micrograph of integrated back-gate device with diamond tip array (left) and schematic cross-sectional drawing (right)

I.A Comparison of Results with Proposal

The 220GHz high power amplifier (HPA) described in the DARPA HiFive BAA requires an electron source that can achieve high current densities (750 A/cm^2) sustainable over 1000 hours of lifetime. Proposed by the team of the International Technology Center(ITC) and Vanderbilt University (VU) was the integration of two of the leading cold cathode technologies, molded diamond tips and the back-gate field-emission devices (bgFED) to achieve these goals. Both technologies generate extremely high current densities, and prototypes devices have already been produced for both. Combining the two technologies provides the benefit of stable high current density diamond tips and the arc-resistant long term performance of bgFEDs. BgFEDs based upon diamond were designed, fabricated and performance evaluated in a collaborative effort between the ITC and VU.

Diamond tip arrays laid out in a geometry consistent with the requirements of the high power amplifiers of the HiFive program demonstrated emission from greater than 90% of the tips in the array. In diode mode a total emission current of ~600 mA at 6.1 A/cm^2 was achieved. This is equal to the highest reported emission current from a field emission cathode. An emission current of 15 mA was achieved at 15 A/cm^2 from 1mm by 0.08mm cathodes designed specifically for this program. This is in comparison to the 250 mA and 750 A/cm^2 goal of the HiFive program. Although, the results are well below those required for the HiFive program, they are among the highest current and current density reported for cold cathodes. The modeling predicts the back-gated diamond tip arrays can achieve the performance required for this program.

I.B Technology Transition Plans

Milestones and deliverables for the 12 month period of performance were identified for the end of each of the two six months periods. Prototypes of the advanced cathode based on back-gated diamond field tip arrays will be completed and tested. The emission tests of the prototype devices will determine the performance level with respect to the goal of achieving a maximum current of at least 0.25A from 1mm x 0.08mm total array area and current density of at least 3A/mm2. At the end of the second six months emission test will be conducted to determine the performance level with respect to the goal of achieving a maximum current of at least 0.25A from 1mm x 0.0.04mm total array area and current density of at least 7.5 A/mm^2.

The proposed back-gate diamond tip array field emission device is based upon the integration of prior technology developed independently at Vanderbilt University and ITC. The patent pending back-gate device geometry was developed by ITC (PA 20050116214). The back-gate device geometry was proposed as a way to solve the historical failure mechanism of gated FEAs, arcing. The elimination of the cavity surrounding the tip as a source of out-gassing and the associated arcs when a high electric field was applied has yielded devices which are robust to handling and testing. Lifetime tests up to 700 hours have been performed with stable continuous DC emission. Vanderbilt University researchers developed an innovative fabrication process [(US Patents 6,762,543; 7,256,535),] for realizing robust diamond-based emitter tips. Ultra-sharp pyramidal diamond microtip arrays with a tip radius of curvature of less than 5nm are routinely achieved, utilizing a silicon mold and diamond chemical vapor deposition. The combination of the back-gate geometry with diamond emission tips will provide a very high current density cathode for RF amplifiers and other applications.

Currently bgFED devices are fabricated on 100 mm silicon wafers that can be processed in lots of up to 20 wafers using existing facilities. Even if the wafers are diced into 1 cm × 1 cm die the number of bgFEDs produced in a single process run is expected to supply a significant fraction if not all of the anticipated demand. The addition of a CVD reactor to deposit diamond

for the emitter tips is the only major manufacturing piece of equipment needed to fabricate the devices using the combined ITC and Vanderbilt University technology. The layout of the mask set can accommodate a variety of designs/dimensions to accommodate different vendor requirements on a single substrate. Once these cathodes meet the program or other customer requirements they will be made available to vendors. Since the demonstrated performance provides among the highest recorded currents and current densities, the cathodes can be used in other high power amplifier designs.

Section II Detailed Results

II.A SOW and Deliverables

The advanced cathode team (VU and ITC) in first 6 months began with establishing a process flow for the fabrication of the diamond back-gate structure; this included photo-lithography mask design and purchase. Prior to finalization of designs, ITC conducted electrostatic modeling to validate the proposed design in terms of anticipated performance (operating voltage, emission current, etc.) In parallel, VU conducted doping studies on diamond FEAs and integrated barrister resistors, including materials characterization. As arrays were made available by VU, ITC began process development, in particular the merging of the as-grown arrays into the back-gate structure. Simultaneously, field emission testing (high current pulsed and DC modes, as well as long term testing) at VU and ITC were planned but only the pulsed test were conducted. The deliverables for this phase included: process flow (including photo mask sets) for the microfabrication of the advanced cathode; data resulting from materials characterization of diamond FEAs and barrister resistors; field emission data summarizing the performance of the diamond based emitters. Efforts continued in the phase for Milestone II (next 6 months), with emphasis on revising and optimizing the fabrication of the diamond FEAs, and the integration of these arrays into the back-gate structure. Field emission testing continued at both VU and ITC, with a focus on determining maximum current and current density; long term field emission test was not conducted as planned. The deliverables for this phase include: optimized device design and process flow (including photo mask sets) for the microfabrication of the advanced cathode; high current field emission data.

Detailed tasks/subtasks included in the proposal to be performed:

(a) ITC

Task 1: Electrostatic Device Modeling

Using commercial software FEMLAB, 3D simulation of the bgFED based on the real tip configuration was performed. It was assumed that tips have 5nm radii and 0.5-1um length of the needle-like top of the tip merging a pyramid. Taking in the account pyramid base 2umx2um and cathode line width 2um field distribution within the system was simulated. Importantly, the local electric field in the vicinity of the top of the tip (emitting spot) generated by different voltage

applied to a back gate, was simulated based on a given macroscopic field generated by an anode. Thus, the field enhancement factor combining geometrical configuration and the back gate effect were estimated and current density from a tip calculated. To be addressed was if the screening effect of the tips take place for the planned inter-cathode line distance (2um). Inter-cathode distance was optimized for the best performance. In addition, an analysis was completed to estimate if the tips on the nearest lines should be shifted and form a chess-board configuration to avoid screening while still maintaining the highest tip density.

Task 2: bgFED Device Design

Device configurations outlined were blue printed based on the results of the electrostatic device modeling.

Task 3: Lithography Mask Design

Lithography masks were drawn and ordered according to the 3 device configurations and 2 types of etching to be pursued.

Task 4: Process Flow Development & Diamond + bgFED integration

After the barrister resistor layer of lightly doped diamond was grown by VU, ITC continued device fabrication by depositing a suitable adhesion layer over the CVD diamond surface to provide a means of bonding the diamond emitters to the back-gate substrate, as well as to provide a conduction path for the diamond cathode lines. Then the diamond emitters were wafer bonded to a conducting silicon wafer with a thin dielectric film (such as n-type silicon with > 0.5 μm of thermal oxide) similar to ITC's back-gate geometry, and controlled etching of the mold wafer was performed until the diamond tips are exposed for alignment purposes. A suitable first etch mask such as Al or Ni was deposited and patterned to protect the diamond emitters during the subsequent silicon and diamond etch. The next step was RIE of the remaining mold silicon and the exposed diamond. After removal of the first etch mask, a second etch mask for the adhesion layer was deposited and patterned. The adhesion layer underwent etching to form patterned cathode lines. Removal of the etch mask and remaining silicon completed the fabrication of the diamond back-gate field emission device with built-in barrister resistor for every pyramidal tip.

Task 5: Lithography Mask for First and Next generation Designs

Based on different tips densities for first and second generation devices, 2 sets of masks (2 etch masks for each set) were to be designed for the device configurations. One more set of masks was required for the edge device configuration for the second generation of devices.

Task 6: Diamond + bgFED integration of next generation device

Process similar to that described in Task 4 was performed for a second generation of the devices.

Task 7. Field emission test

The fabricated bgFED will be tested using the International Technology Center's test chamber which allows for the measurement of 7 samples/per batch; all of the samples in a batch will be subjected to the same history of exposure to the residual gases in the test chamber. This guarantees measurements with high yield (since there is no pumping time between sample measurements) and repetitiveness. The sample holder in the ITC test chamber was adapted to a triode configuration by simply providing an extra contact to the top cathode of the sample insulated from the contact to the bottom gate. In the ITC test chamber the following tasks are already automated: control of the anode-cathode gap, sample position, IxV curves, SI plots, current x pressure curves and current x time curves. The triode measurements focused on determining the current x gate voltage curves for a given anode voltage and distance, while the long term stability was focused on the current x time and current x pressure curves. Long term measurements as long as 200 hundred hours of emission were be made, and they were to serve as a preliminary indicator of the device suitability for the applications.

(b) Vanderbilt University

Task 1: Develop mask & fabrication flow of diamond field emitter arrays (FEA).

Subtask 1.1: Diamond field emitter array masks.

Figure 3 below shows 3 types of diamond field emitter array mask configurations implemented in this project. Array configuration (a), designed for Milestone I study, uses array with 2umx2um base width and array-array separation of 2um (i.e., tip-tip separation of 4um) over a real estate of 0.08mm^2 targeted to obtain a current density of 3A/mm2. With the help of bgFED and barrister resister enhancements, this configuration was estimated to provide up to a total emission current density of 6.3A/mm^2 and current of 0.25A. Array configuration (b), designed for the Milestone II study, is similar to (a) but with the tip-tip separation reduced to 2um and real estate area reduces to 0.04mm^2. This configuration can provide according to projections a total emission current density of up to 12.6A/mm^2 and current of 0.5A, which exceed the requirements of HiFive. While theoretical projected values were relatively high, we targeted as our milestones the current density characteristics required for the HiFive program. Array configuration (c) is similar to (b) but using edge emitter with base dimension of 2umx40um, instead of 2umx2um square, aimed to draw much higher current.

Subtask 1.2: Fabrication of diamond field emitter arrays.

The mold transfer process for fabrication of diamond field emitters is an efficient technique to create well-controlled and uniform emitter tips over a wide area. A process has been

developed to precisely pattern pyramidal polycrystalline diamond tips on diamond by this method. Using this process it is possible to control and optimize the sp2 content, surface treatment, and boron doping of the diamond tip in order to improve their field emission behavior. This well-developed technique was employed in this project. Diamond field emitter arrays were fabricated from chemical vapor deposition (CVD) deposited in and on the silicon mold, per the mask-designed. The CVD fabrication parameters will be adjusted to control the sp3/sp2 content in the diamond film. Boron doping will be achieved in-situ from a boron source during diamond deposition.

Task 2: Doping adjustment on barrister resistor arrays and diamond FEA

The boron doping concentration in the diamond FEA and barrister resister layer was controlled during in-situ CVD diamond depositions. The doping concentration of the fabricated diamond layers was measured by secondary ion mass spectrometry (SIMS) and/or Rutherford back scattering. The resistivity of the diamond film and barrister resister layer was characterized and measured.

Task 3: Develop fabrication process of built-in diamond-based barrister resistors

The critical step in the fabrication of built-in diamond-based barrister resistors is the masking and etching of the diamond cathode material using reactive ion etch (RIE). The micro-patterned diamond barrister resistors were fabricated using an O_2 plasma using an STS Advanced Oxide Etch (AOETM) ICP-RIE system. The aluminum mask layer offers high etch selectivity. A coil/platen R.F. power of 700W/150 W with a 30 sccm oxygen flow rate at a pressure of 10 mTorr was used. Experience predicted that the barrister resistor structures as designed would be achieved.

Task 4: Material/physical characterization of barrister resistors and diamond FEA

The microstructures of barrister resistors and diamond FEA were examined by scanning electron microscopy (SEM). The radius of curvature at the tip apex will be measured. Uniformity in size and shape of the diamond tip array was examined. The quality of diamond film, sp3/sp2 (diamond/graphite) composition, was characterized using Raman spectroscopy. The relative height of sp2/sp3 served as a qualitative comparison of sp2 incorporation into the diamond films, considering sp2 bonding has about 50 times higher scattering efficiency than sp3 bonding.

Task 5: Test diamond FEA for high current RF at pulse and DC modes

Field emission testing of the bgFED was performed in a vacuum chamber of 10^{-6} Torr that provided a sufficient vacuum environment for device characterization in DC and pulse modes. The emission test system available at VU is also equipped with computer controlled electrical measurement interfaces. The emission current of the bgFED was measured as a function of gate and anode voltages in DC mode. Emission in pulse mode was characterized as a

function of pulse frequency, amplitude, and duty cycle. The emission data obtained from the diamond tips was analyzed by the Fowler-Nordhiem equation.

Task 6: Determine Jmax, Itotal , and stability of diamond FED for 1000 Hrs life.

The maximum emission current, and current density and life time were investigated for a set of bgFED fabricated with respect to the proposed designs outlined in Task 1. The effects of array geometry/configuration on the FED performance were examined with the goal of achieving the performance requirement as specified by HiFive program.

Task 7: Enhance current handling capabilities and minimize energy/power loss

Emission enhancement attributes by the back-gate design to allow the bgFED to operate at lower field, higher current and suppression of arcing were studied. The effect of the built-in barrister resister that allows real-time self-adjustment of the emission current for individual tip to ensure current uniformity over the array were examined.

Task 8: Design and fabricate advanced diamond bgFEA

The final refinement in design and fabrication of the advanced diamond bgFED were to be based on the results obtained from tasks 1-6 and ITC. Final diamond bgFED will be fabricated.

Task 9: Determine Jmax , Itotal , and modulation frequency of bgFED

The diamond bgFED performance at HiFive Specifications (Jmax=750A/cm2, Itotal = 250mA, life-time=1000hrs.) at a given duty cycle were to be examined.

ITC/VU final task

Final Task: Deliver prototypes to government research labs for further evaluation.

Deliver diamond bgFED to HiFive partners for evaluation.

Deliver final report.

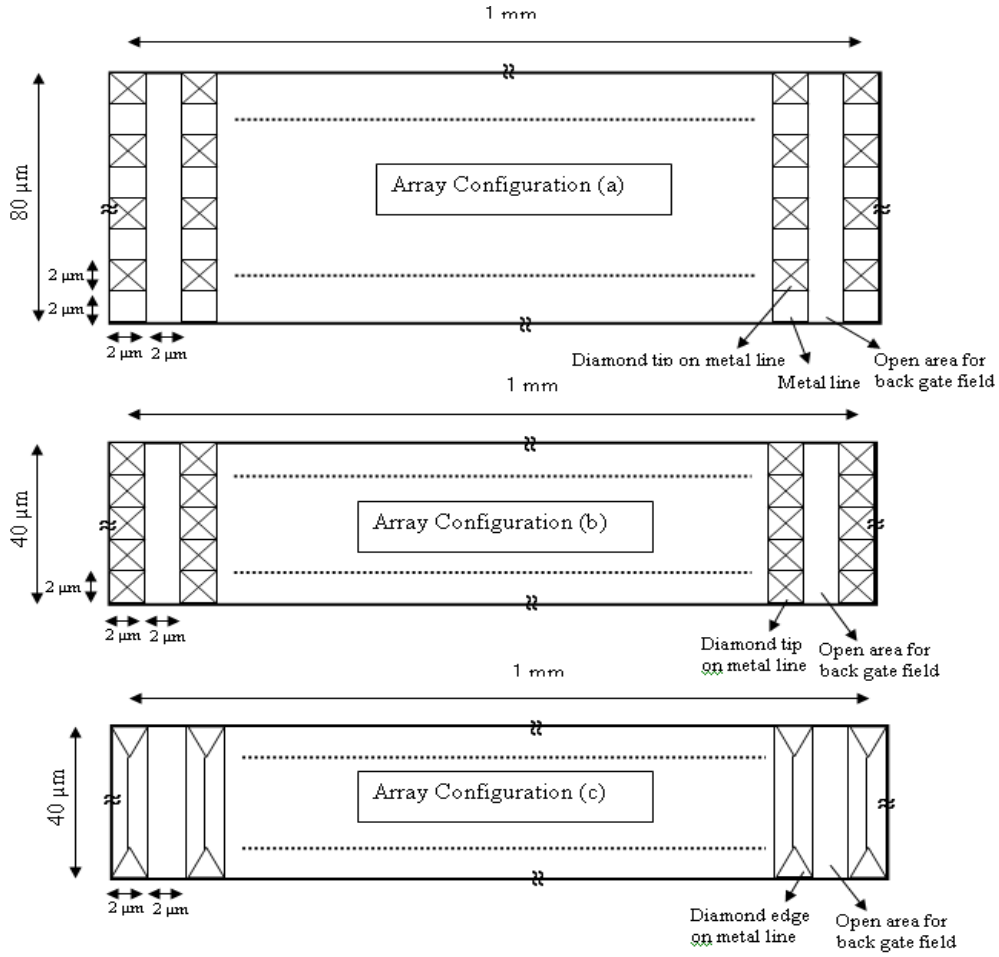


Figure 3: Proposed field emission array configurations

II.B Back Gated Field Emission Device Final Approach

II.B.I Finite Element Modeling of Tip Array Performance

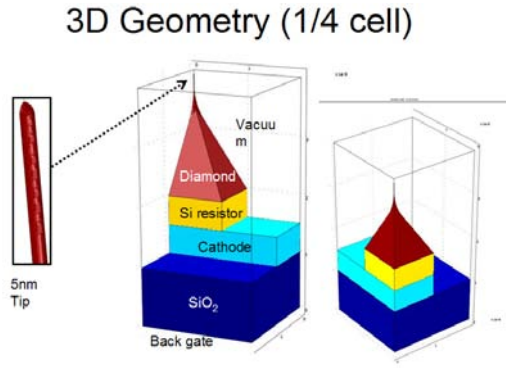


Figure 4 Simulation cell for the diamond bg-FEA. Thicknesses: SiO_2-0.5um, cathode-0.5um, ballast resistor- 0.5um. Entire cathode assumed conductive.

Diamond emitting structures for both wedge and tips configurations were developed in the project. To optimize the performance of the diamond bg-FEA, electrostatic modeling of the realistic geometries (i.e. within the range of the available microfabrication capabilities, Figure 4 has been evaluated using the Finite Element Analysis (FEA) package COMSOL 3.5a. Due to disparate dimensional mismatch between the overall device dimensions and the active emission location at the diamond tip, r=2.5nm, a geometrically multi-scalar

approach was taken whereby the computational domain was broken into four regions, three 3D and 1D, such that a correlation between macroscopic device scale effects and electron emission behavior at the diamond tip is possible. Potentials coupled from coarse levels to succeeding fine levels at boundaries (4 mesh levels; mesh size at tip apex < 1 Å).
Statistics of typical simulation run:

(1) Computer used : Asus G1S Laptop with 2GHz Intel Core2 Duo T3700 CPU, 2GB DDR2 RAM, NVIDIA GeForce 8600M GT, Windows XP Professional;
(2) FEA Simulation model: (i) 96000 DOFs, 4 geometric layers to model, three 3D and one 1D, to model disparate length scales, (ii) approximately 3000 node points per geometric layer; (iii) approximately 50 node points/nm across the tip apex in 1D model, (iv) quadratic Finite Elements, (v) 110 discrete loops through FEM subroutine, (vi) 11 Voltage Steps, (vii) 10 Spatial Steps, (viii) simulation time required – 900-110 seconds.

A routine was created to calculate all current densities & current per tip within Femlab from boundary integrals using local fields from the modeling and the Fowler-Nordheim equation. The local field on the emitter was determined for a given back-gate voltage and device geometry. The space charge effect was not included.

Optimization parameters included: (i) pitch between cathode lines and between tips along cathode lines to reduce back-gate field screening and increase current density for each wedge/tip; (ii) line density to increase the number of emission sites within cathode area and (iii) height between back gate and tips for effective electric field modulation. The recommended pitch between cathode lines obtained from the modeling for wedges with 2µm base is 7-10 µm. For the wedge structure a total predicted current increase of 3x after applying 100V to the back-gate at a macroscopic field (from anode) of ~25V/µm, thus indicating noticeable current modulation with a back-gate.

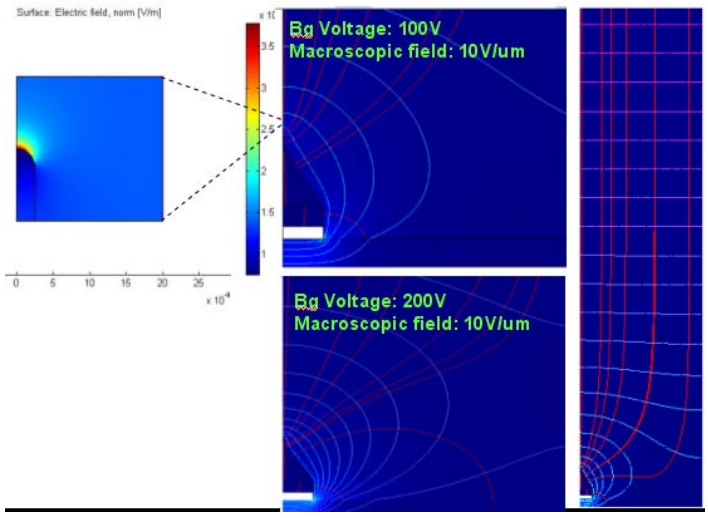


Figure 5 Electric field (left) and electric field streamlines (right) for the Bg-tip array wedge structure at different macroscopic fields and Bg voltages.

Beam divergence is an important characteristic and needs to be addressed separately (through electron trajectory simulations which were not included in the SOW for the current project). However, based on field streamlines (Figure II.B.I.2), the majority of electrons should emit toward the anode at certain back-gate voltages.

Besides, at later stages of the project the decision was made to remove the dielectric from the central part of the inter-cathode lines area, further minimizing charge build up in the dielectric of the back-gate from electron bombardment.

Simulations demonstrated significant geometrical local field
ıll radius at the end of a pyramid. For a

tip array, with 4um pitch between tips along cathode line and 8 µm between cathode lines, the field enhancements at the tip were ~100 for gate voltage of 0V. After applying a gate voltage of 100V field enhancement increased up to ~140, what is anticipated to result in a significant increase in the current density. Figure II.B.I.3 illustrates the current density from the cathodes depending on the back-gate voltage for two values of work function: 4.5eV and 4.0 eV. As can be seen from the figure, back-gate modulation can provide x100-1000 enhancement of the current from a tip depending on the work function of the diamond material (which can be lower than 4.5eV typical for bulk diamond samples due to specific microstructure of the material (nanometer sized grains and small amount of sp^2 phase within grain boundaries). Thus, based on the modeling results and assuming perfect fabrication of the structure, the program goal of 7.5A/mm2 theoretically can be achieved (especially if the work function of the tip is below 4.5eV)

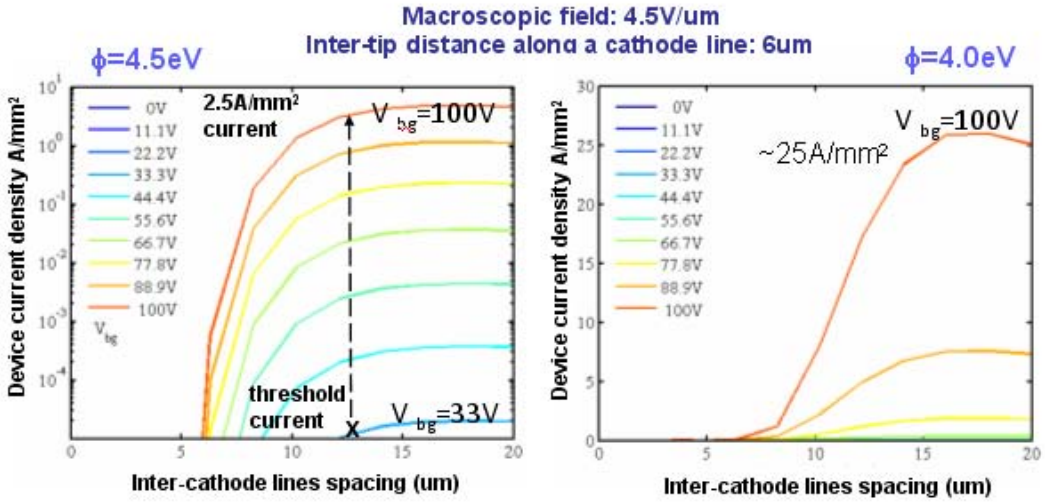


Figure 6. Schematic illustration of the predicted current modulation at different back-gate voltages as a function of inter-cathode line spacing at two different work functions.

Below is a summary of the predicted geometries (for highest current density).

<u>Pyramid base: 2.0x2.0µm</u>

- Back-gate to tip apex distance 3.4µm
- Inter-tip pitch along cathode line 5-6µm
- Inter-cathode line pitch 12-15um

(14,000 tips per mm^2)

<u>Pyramid base: 1.5x1.5µm</u>

- Back-gate to tip apex distance 3.05µm
- Inter-tip pitch along cathode line 4.4µm
- Inter-cathode line pitch ~10um

(22,700 tips per mm^2)

II.B.II Diamond Tip Array Fabrication

Diamond FEAs were fabricated using the mold transfer technique (US patent # 6,132,278) developed at Vanderbilt University. The molds were fabricated by patterning the mask design on silicon-on-insulator (SOI) substrates and by subsequent anisotropic etching of the (100) silicon wafers. The resulting inverted pyramidal cavity is defined by the slower etching {111} planes of silicon that form the sidewalls of the cavity. The tip of the mold was further sharpened by thermal oxidation. Sharpening happens because the thermal oxidation rate on the (111) planes of the inverted pyramidal/edge surface is faster than that on the (100) plane of the silicon base and the oxidation rate at the inverted apex is the smallest due to limited oxidation reaction in this confined region. It is beneficial to sharpen the pyramidal diamond tips to achieve the highest field enhancement at the tip and subsequently the highest electron emission. A SEM micrograph of an inverted pyramidal mold is shown in Figure 7. Figure 7a shows a cross-sectional schematic view of the inverted pyramidal mold on a silicon substrate. The SEM micrograph of Figure 7b reveals the details of the fabricated mold with a 2μm tip-base.

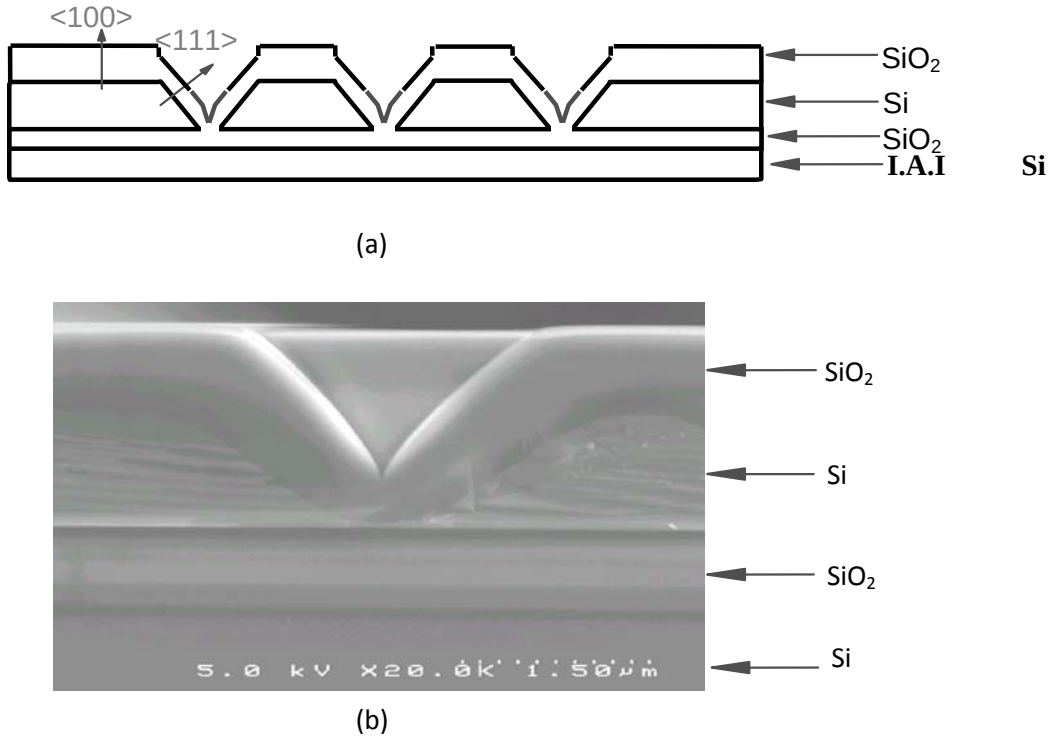


Figure 7: Cross-sectional schematic (a) and SEM micrograph of mold with 2μm tip-base for the formation of diamond tip arrays (b)

a) Fabrication of Diamond for bg-FEA:

Figure 8 shows the fabrication flow chart for achieving diamond tip arrays.

- Define FEA dimensions/configurations and construct mold structures on SOI substrate.
- Perform thermal oxidation for mold sharpening
- Deposit diamond into SOI molds
- Give the fabricated diamond FEAs to ITC for subsequent back-gate integration, otherwise Vanderbilt proceeds with the following fabrication steps to complete diamond FEAs without back gate integration
- Perform high temperature diamond brazing on Mo substrate
- Perform backside silicon etching until etch-stopped at the buried oxide
- Perform oxide and silicon etching

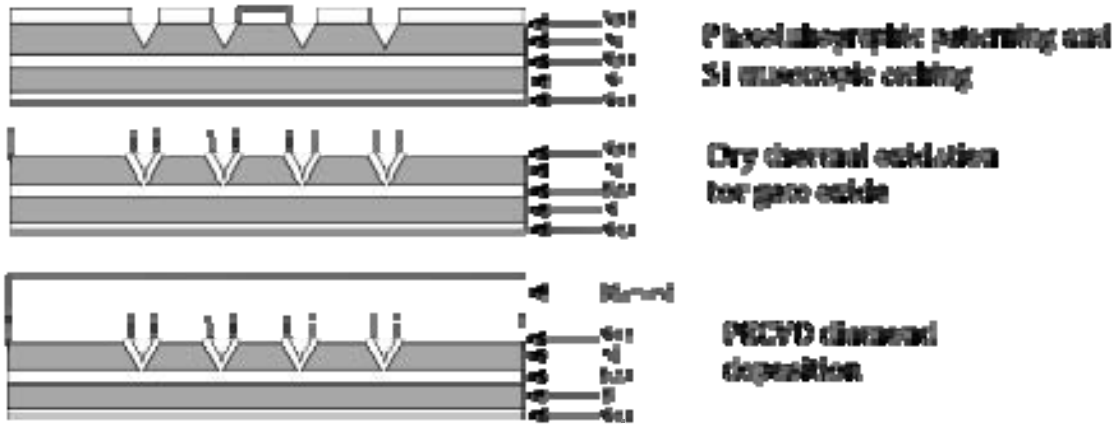


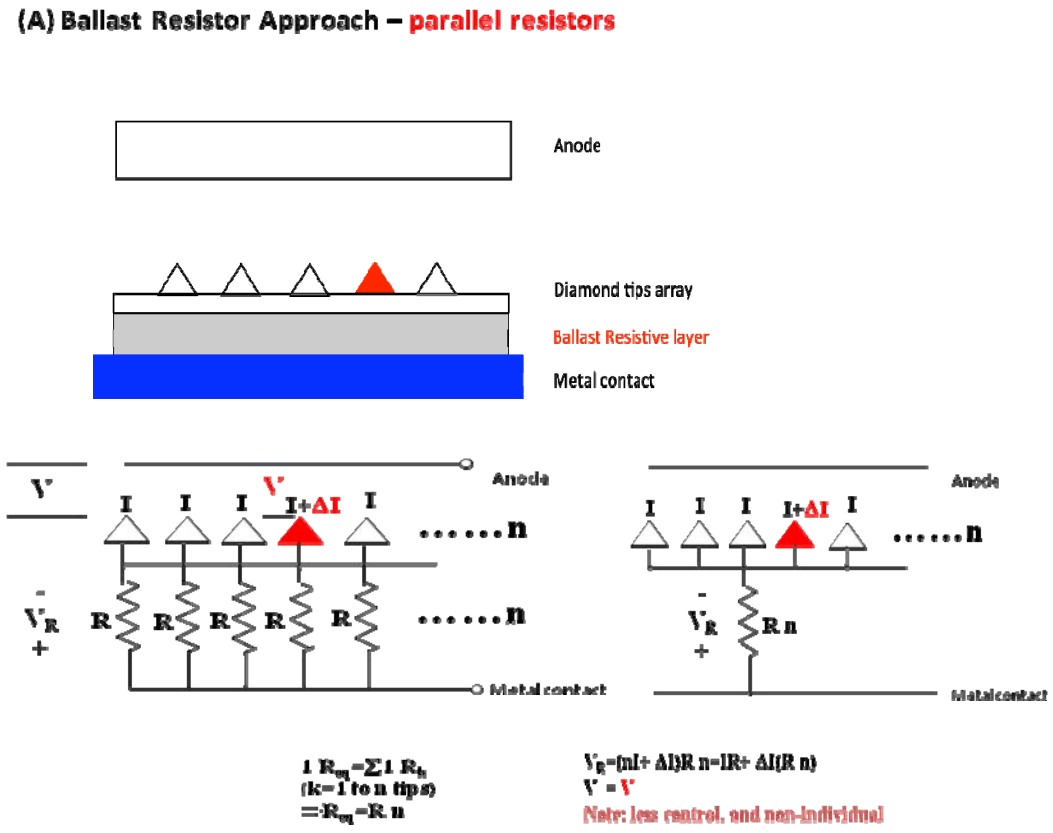
Figure 8. Schematic of fabrication flow performed to form diamond arrays.

b) Doping adjustment on barrister resistor arrays and diamond FEA

A ballast/barrister resistor layer of lightly doped diamond has been incorporated onto the diamond FEA during a 2nd step of the CVD process. Ideally, the use of built-in or integrated barrister resistor with the cathode allows self-adjustment of the emission current for individual tips in real time thereby diminishing non-uniform current concentration in only a small number of tips in the array. Hence, the barrister layer ensures current uniformity over the array by limiting individual tip current (also preventing tip burnout) and allowing non-emitting tips to reach a field strength high enough to initiate emission and equalize the emitting current with other emitting tips, hence enhancing uniform emission over a large area. Two types of resistor

incorporation schemes have been envisioned (see Fig. 9): (A) a more conventional ballast resistor approach where all tips sit on a common resistive layer (parallel resistor configuration) hence less effective, and (B) a more advanced barrister resistor approach where each tip has its own resistive layer (non-parallel configuration) hence more effective but harder to make.

The ballast resistor approach was implemented and FEAs implemented using this approach demonstrated more uniform emission over the entire array for the diamond FEA in diode testing. However, the realization of the 2nd approach depends on the realization of the final bg-FEA, which includes the isolation of the resistor from individual tip in the final fabrication process.



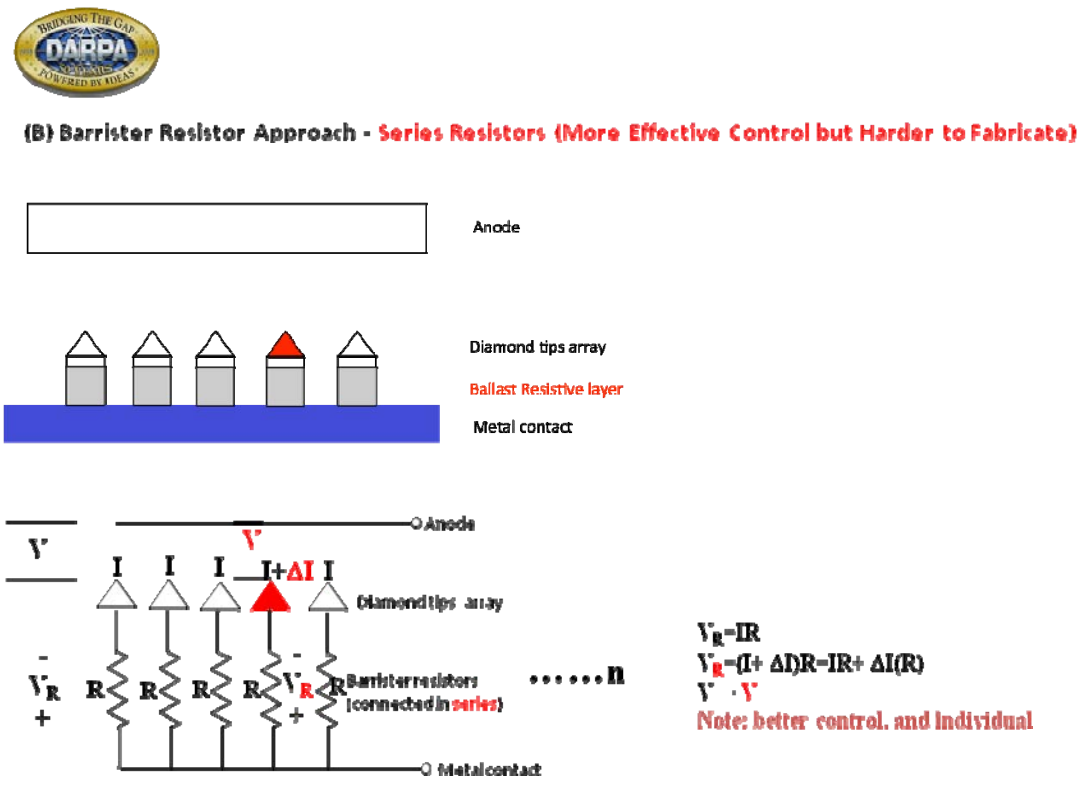


Figure 9: Built-in resistor approaches, (a) ballast resistor and (b) barrister resistor

c) Develop fabrication process of barrister resistors and diamond FEA

Diamond FEAs were fabricated by the mold transferring method, which produced well-controlled diamond emitters with a well-defined microstructure and uniformity over a large area. Thermal oxidation of the Si of a SOI wafer with 1-μm BOX was performed, then patterned followed by etching of the oxide through which the Si is anisotropically etched forming the pyramidal mold. The silicon substrates were processed per the Vanderbilt process and the molds created preparatory to diamond deposition.

Subsequent operations were performed to achieve the diamond emitter arrays. In the mold transferring technique, a cathode structure is produced by deposition of the cathode material into the mold having an inverse shape of the cathode geometry. We have successfully fabricated diamond pyramidal microtips (Fig. 13) and micro-knife-edges (Fig. 14) by a 2-step PECVD diamond deposition process into inverted pyramidal/edge silicon cavities, respectively.

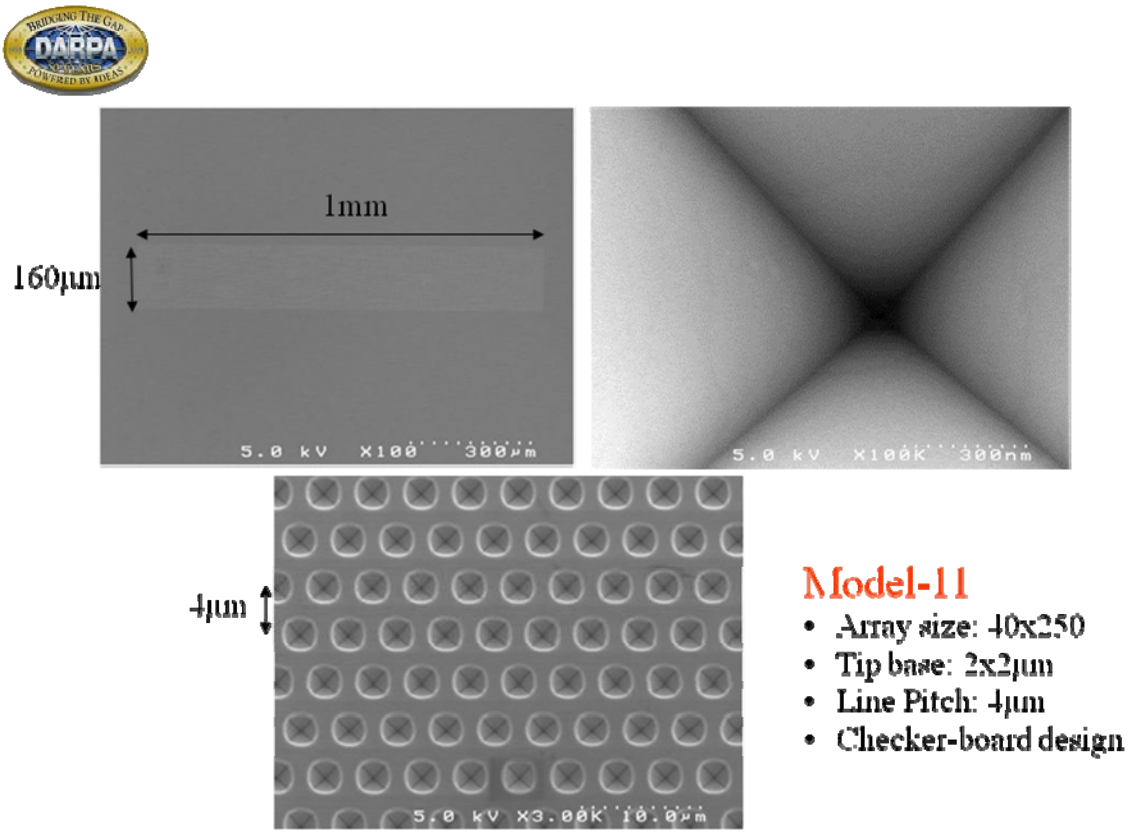


Figure 10: Etched cavity pyramidal emitter Mold

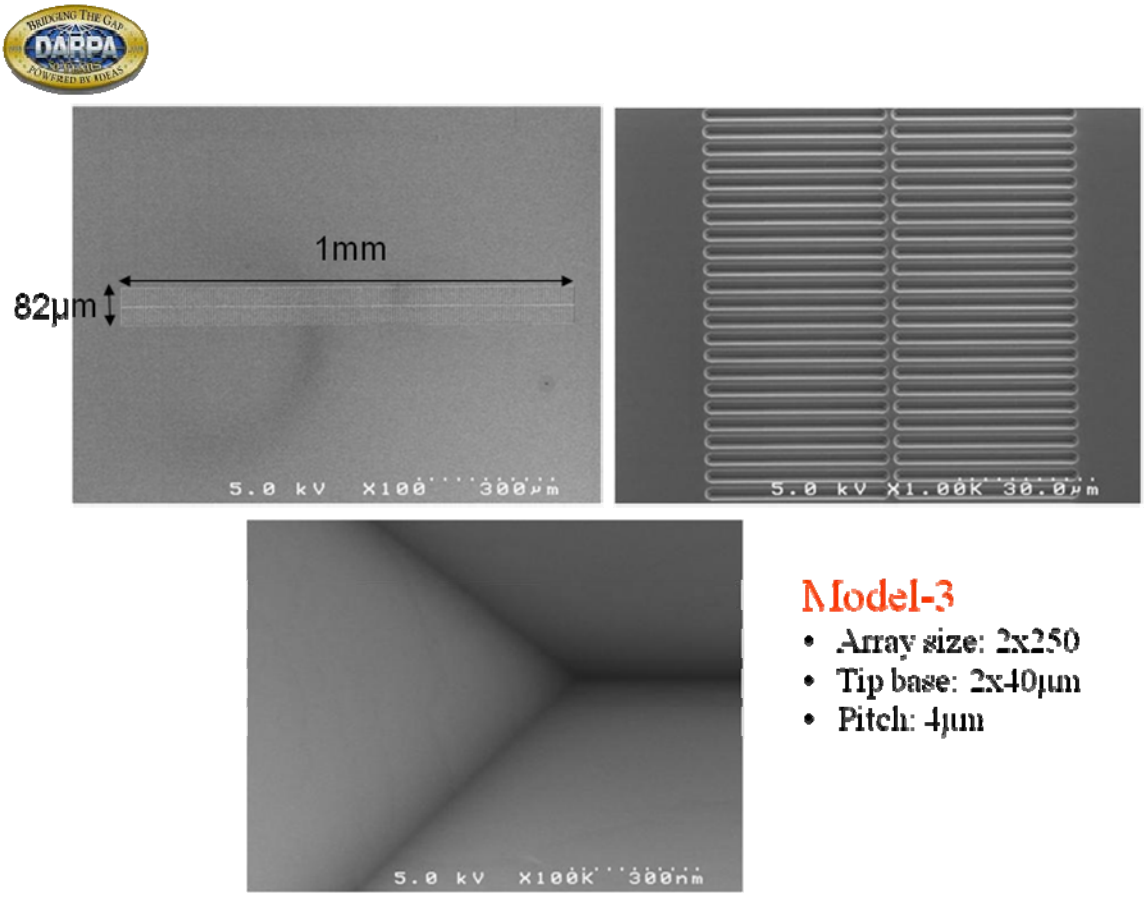


Figure 11: Etched cavity wedge emitter mold.

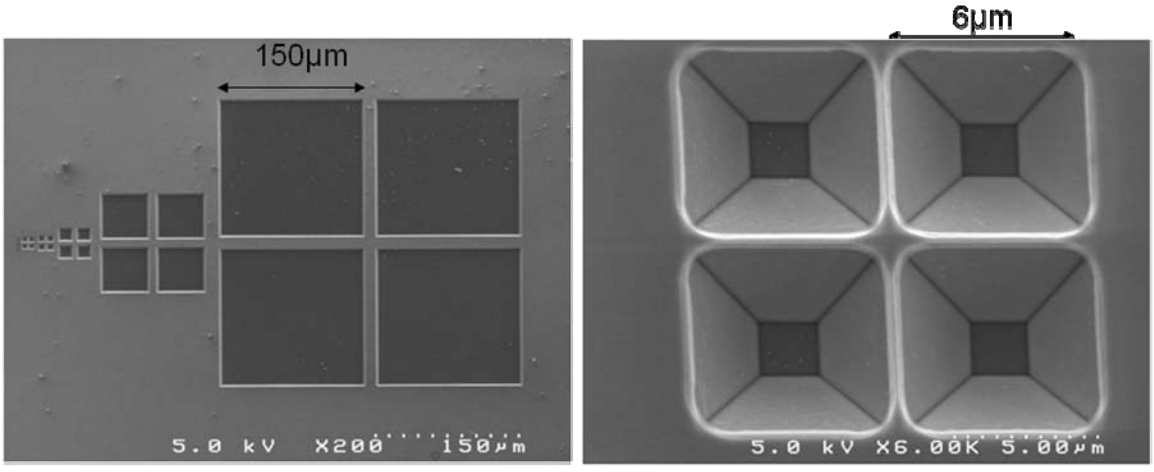


Figure 12: Etched cavity alignment marker mold.

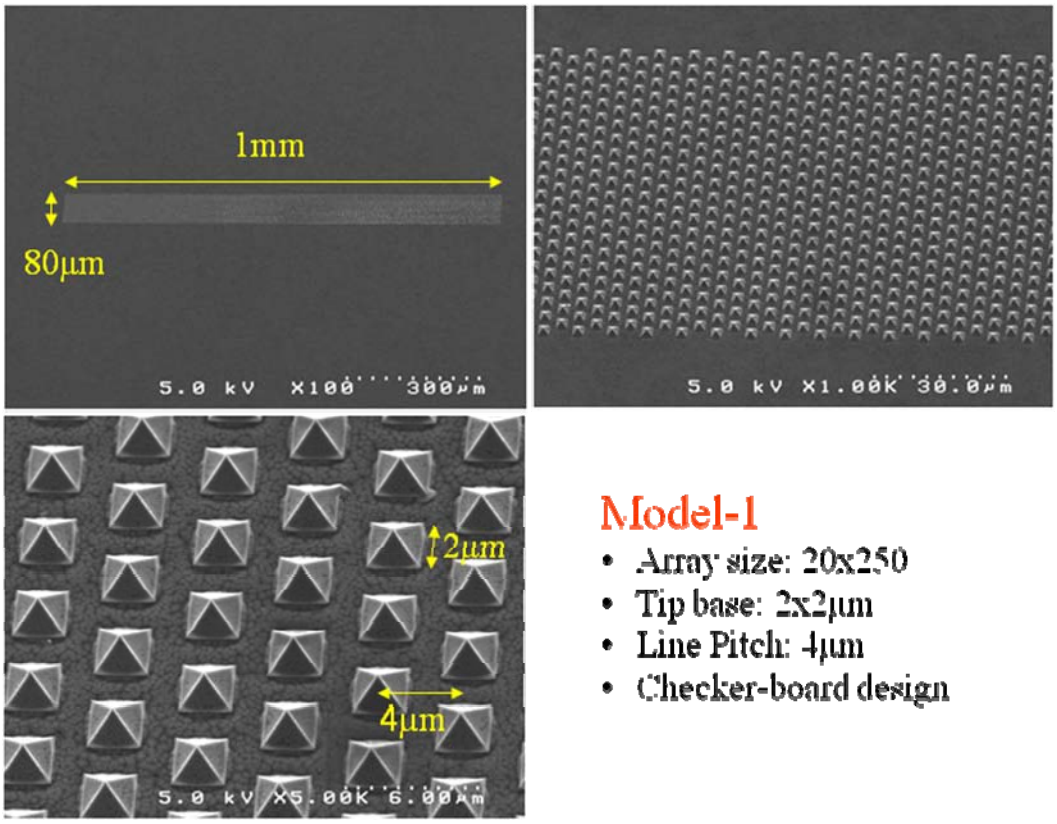


Figure 13: SEM micrograph of fabricated diamond pyramidal FEAs.

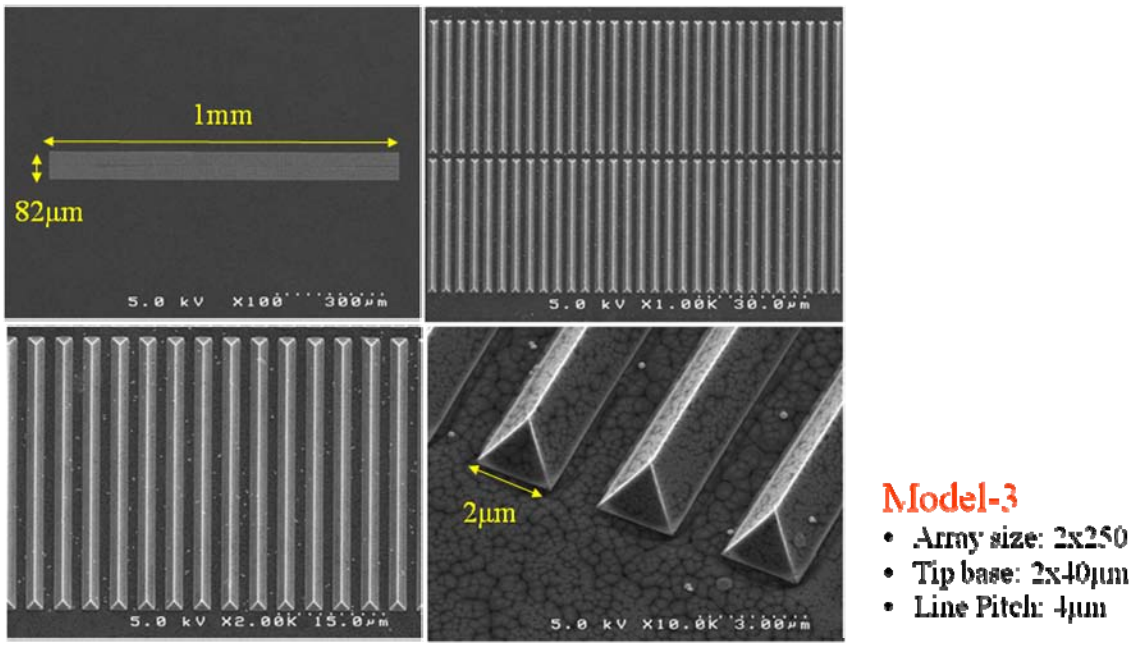


Figure 14: SEM micrograph of fabricated diamond edge FEAs.

d) Material/physical characterization of barrister resistors and diamond FEA

The microstructures of the fabricated diamond field emitters were examined by SEM) and their sp^3:sp^2 content were characterized by Raman spectroscopy. SEM micrographs of pyramidal diamond tips and knife-edges at different magnifications are shown in Fig. 15 and 16, respectively. The detailed topology, geometry, and dimension of a single diamond tip shows a pyramid with a base dimension of 2 μm x 2 μm and a tip radius of curvature <10 nm measured using a high magnification SEM. For the diamond micro-knife-edge array, it also can be seen that the diamond field emitter is comprised of polycrystalline structures separated by grain boundaries. The SEM images also reveal that ultra-sharp diamond tips/edges with good uniformity in size and shape can be reproducibly fabricated by the mold sharpening transfer technique. The fabrication of ultra sharp diamond tips/edges by this method is more practical and economical than other techniques that utilize special etching processes, because the ultra sharp diamond tip/edge geometry can be uniformly controlled and no additional tip sharpening process is required after tip/edge formation.

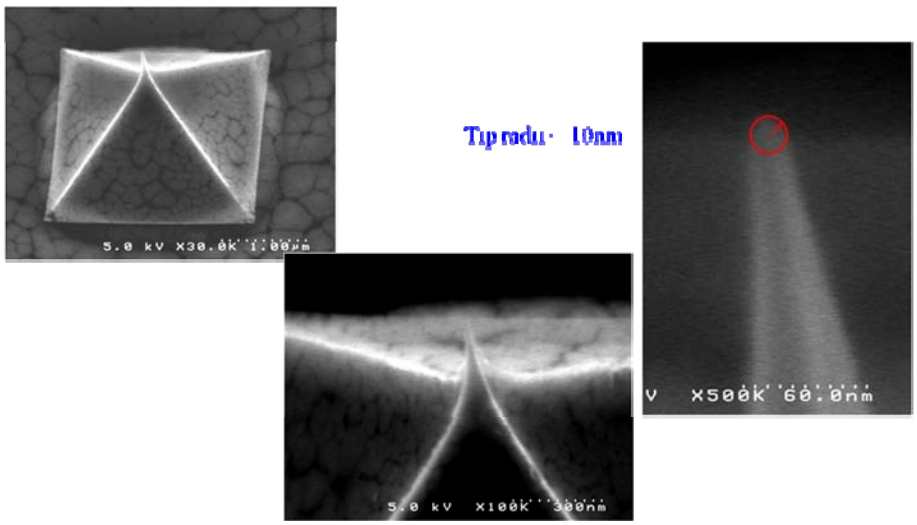


Figure 15: High magnification SEM showing microscopic structures diamond tip emitter

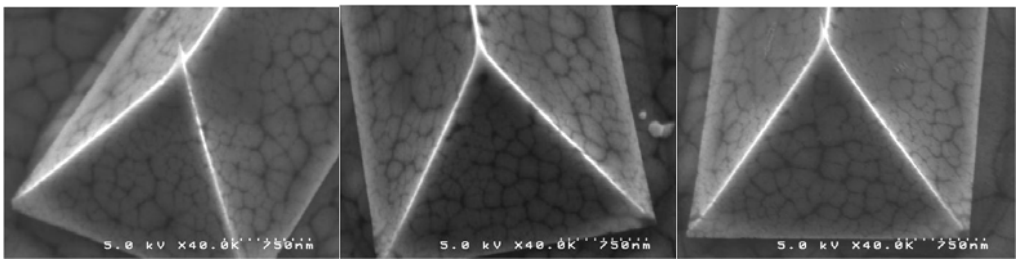


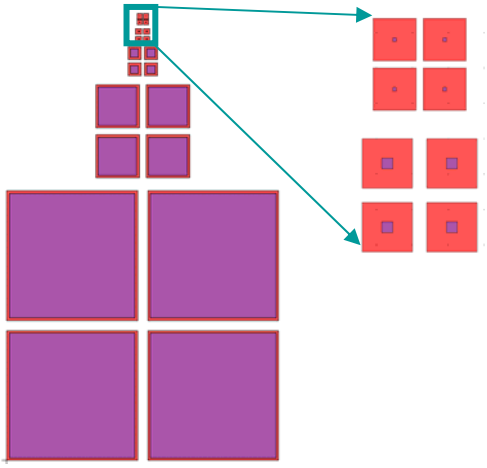
Figure 16: SEM micrographs showing microscopic structures of diamond edge emitter.

II.B.III Back-Gate Integration with Tip Array

Fabrication of the integrated back-gate field emission array (bgFEA) starts with the as-grown diamond tip array from Vanderbilt University (VU). Since the array of tips is formed by depositing diamond into molds formed in the thin device Si layer of a silicon on insulator (SOI) wafer, following deposition the emission tips are buried and a planar diamond surface is the exposed side of the sample.

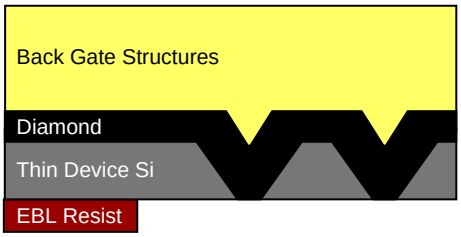
The next step in the initial fabrication method was to coat the diamond surface with metal, using that metal to bond the diamond on SOI wafer to a second substrate, removal of the bulk silicon from the SOI wafer and patterning the diamond. Patterning the diamond requires use of electron beam lithography (EBL) due to the small substrate size (limited by the diamond growth process) and small feature size. In this process, alignment marks included on the front surface of the thin device Si layer must remain after the bulk Si layer has been removed. A series of anisotropically etched pits were formed concurrently with the molds for emission tips were incorporated into the layout as alignment marks. These marking pits were designed to be etched completely through the thin device Si layer, stopping at the buried oxide layer (BOX) of the SOI wafer. The square opening formed at the thin Si-BOX interface would then be used as the alignment marks when the bulk Si and BOX have been removed from the SOI wafer after bonding. Figure 17 shows the layout of the marks and their original intended usage.

Design



- 5 sets of square markers with 150, 50, 15, 7, and 6 µm etch openings.
- Red squares are etch pit openings at the top of the thin Si layer of SOI
- Purple squares are openings formed at the bottom of the thin Si layer of SOI.

Intended Use



Cross section view

Bottom view

- Alignment marks to be used after etching through bulk Si and BOX
- Position of exposed diamond boxes would be used to align EBL pattern at tips

Figure 17: Design and intended use of alignment markers.

Several attempts were made to form metal-to-metal bonds, as well as gold-to-silicon eutectic bonds. Successful bonding was not achieved. This was attributed to the relatively high temperature required while simultaneously applying pressure as well as the difference in the thermal coefficient of expansion (TCE) of diamond with respect to the TCE of the surrounding materials. So, alternative fabrication approaches were investigated. It was decided that a direct fabrication sequence could be used to form the bgFEA structure for this program.

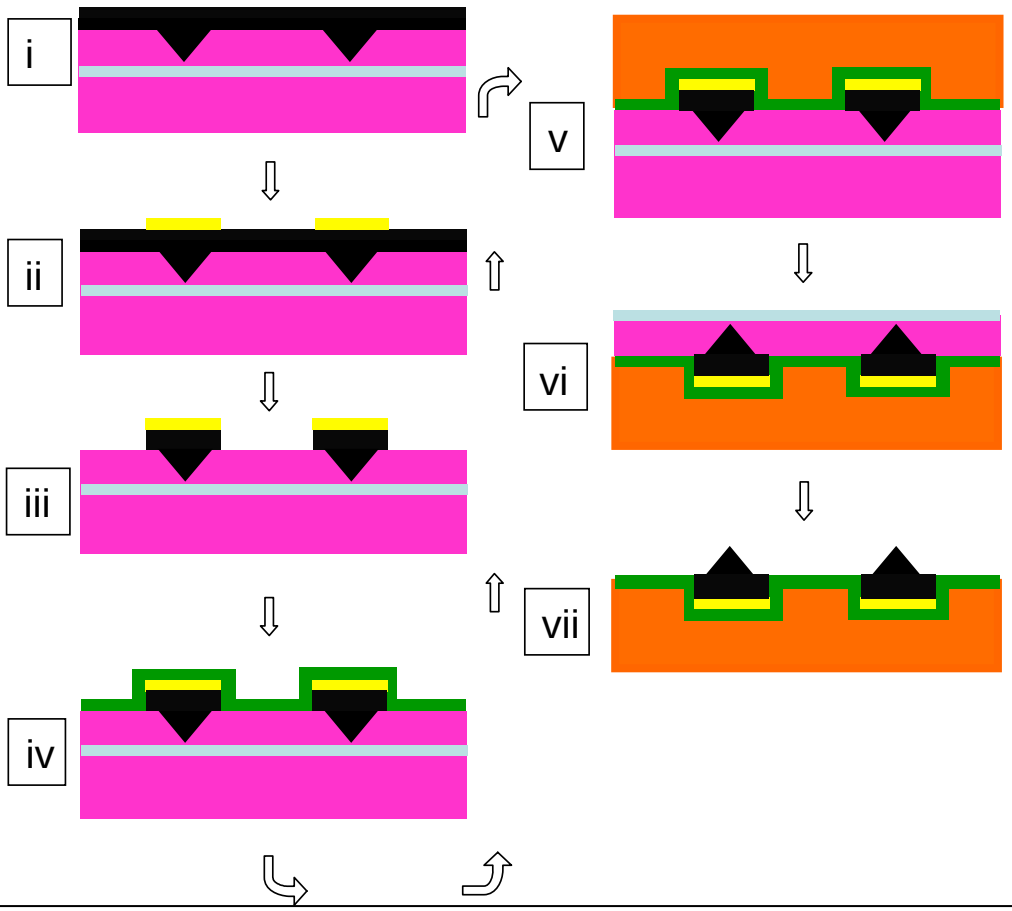
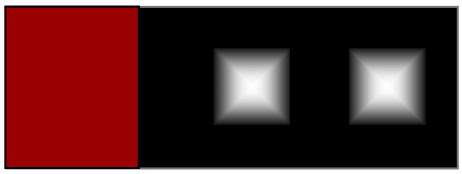
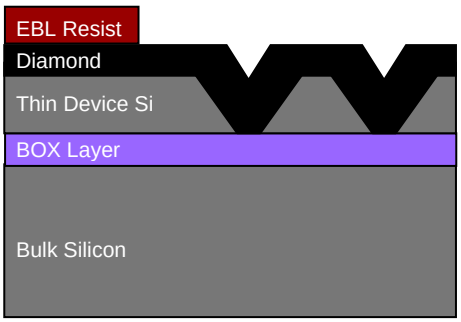


Figure 18: Cross-sectional schematic views of fabrication steps used in the process flow.

The fabrication sequence is shown schematically in Figure 18. It starts with the as deposited diamond tips in the SOI molds (i). The emission lines of the cathode are patterned via EBL and gold cathode lines are deposited onto the substrate (ii). By making the EBL patterning the first step of the process, changes occurred in the way the alignment marks were used. The actual usage of the alignment marks is shown in Figure 19. Use of the marks from the diamond coated side, as shown in Figure 19, resulted in some difficulty at first. As the SEM image in Figure 19 shows, finding the center of the pit at high magnification was problematic as the corners of the pit move out of the field of view.



Top view



Cross section view

- Alignment marks before removal of SOI layers
- It is necessary to find the edge of etch pit features after the diamond layer has been grown

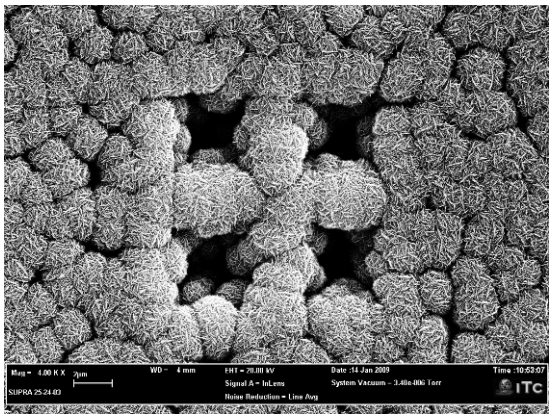


Figure 19: View of alignment marks before and after diamond deposition.

The gold cathode lines cover several tips each, and extend well beyond the edge of the tip array. In addition to carrying current to the emission tips in the final device, the gold lines serve as the etch mask for the removal of the bulk of the diamond material during processing (Figure 18 (iii)). The only diamond that remains on the sample following etching is along the cathode lines and in the emission tips.

After the diamond has been etched, a contact electrode is fabricated using a lift-off step. The electrode contacts the extensions of the cathode lines, joining them together, and extends beyond the tip array. This extension allows the finished device to be wire bonded once the device is mounted in a package in such a way that the wire bond does not interfere with the testing set up. Formation of the bond pad is not explicitly shown in the schematic of Figure 18, but takes place between steps iii and iv.

Once the cathode lines and contact pad have been formed, the next step is formation of the dielectric layer. This is shown in Figure 18 (iv), where the dielectric is shown as the green layer deposited over the top surface of the sample. The dielectric was initially silicon dioxide, but that proved incompatible with the final etching steps. The diamond is deposited in a layer of thermal oxide, which is the final layer to be removed to free the tips. When the dielectric was silicon dioxide, there was no etch stop between these two layers, and freeing the tips without etching the dielectric was not possible. When silicon nitride was used as the dielectric, it provided a suitable etch stop for the final etch step. The electrical properties of silicon oxide and

silicon nitride are similar enough that this change did not have any detrimental effects on the expected operation or performance of the bgFEA devices. The silicon nitride dielectric was deposited by plasma enhanced chemical vapor deposition to give a conformal coating. A conformal coating is required to maintain good electrical isolation between the cathode metal and the back gate metal in all areas of the device.

After the dielectric layer was formed, the next step was formation of the back-gate. Since the bulk Si of the original SOI wafer is to be removed, the back-gate material must be thick enough to provide mechanical stability for the sample. The back gate formation starts with the deposition of a copper seed layer. After the seed layer is formed, the full back gate is formed by electroplating copper onto the seed layer. This thick copper now forms the back-gate of the bgFEA device (Figure 18 (v)).

Once the back-gate has been formed, the diamond tips are freed. This involves removal of the bulk silicon, the buried oxide layer, the thin device silicon layer, and the thermal oxide layer used to sharpen the tips. Bulk silicon removal can be accomplished by several methods. Initially, a wet etch bath of tetramethylammonium hydroxide (TMAH) was used for this step, a process ITC has used successfully in the past. However, the presence of the back-gate material deposited onto the sides of the sample introduced changes to the etch process. The bulk etch proceeded more quickly down the sides of the sample, near the back-gate metal. The TMAH etch mechanism is electrochemical in nature, so it is possible that the metal provided excess electrons to accelerate the rate near the edges. In any event, once the bulk Si was cleared away along the sides, the etch bath attacked and undercut the remaining layers. This led to delamination of the diamond layers as well as the contact pads, resulting in failure to produce completed devices.

Two other etch techniques did prove successful. Both started with trimming the excess metal from the sample sidewalls using a dicing saw. After that, deep reactive ion etching (RIE) using SF_6 as the etch gas, and mechanical grinding were used successfully in removing much of the bulk silicon. Once that was complete, a shorter etch in the TMAH bath was successful in selectively removing the rest of the bulk Si, leaving the BOX, device Si, and thermal oxide layers (Figure 18 (vi)).

TMAH does etch silicon dioxide, but at a much slower rate than silicon. Given this fact, any non-uniformities present in the bulk Si etch would be transferred to the BOX etch. However, the BOX layer is etched using buffered oxide etch (10:1). Since this etchant has no affect on silicon, the device silicon layer served as an excellent etch stop layer, as well as an excellent way for the exposed surface to be planarized.

After the BOX layer was etched, the device Si layer was etched, again in a TMAH bath. Removal of this layer exposed the textured surface of the thermal oxide grown in the Si mold.

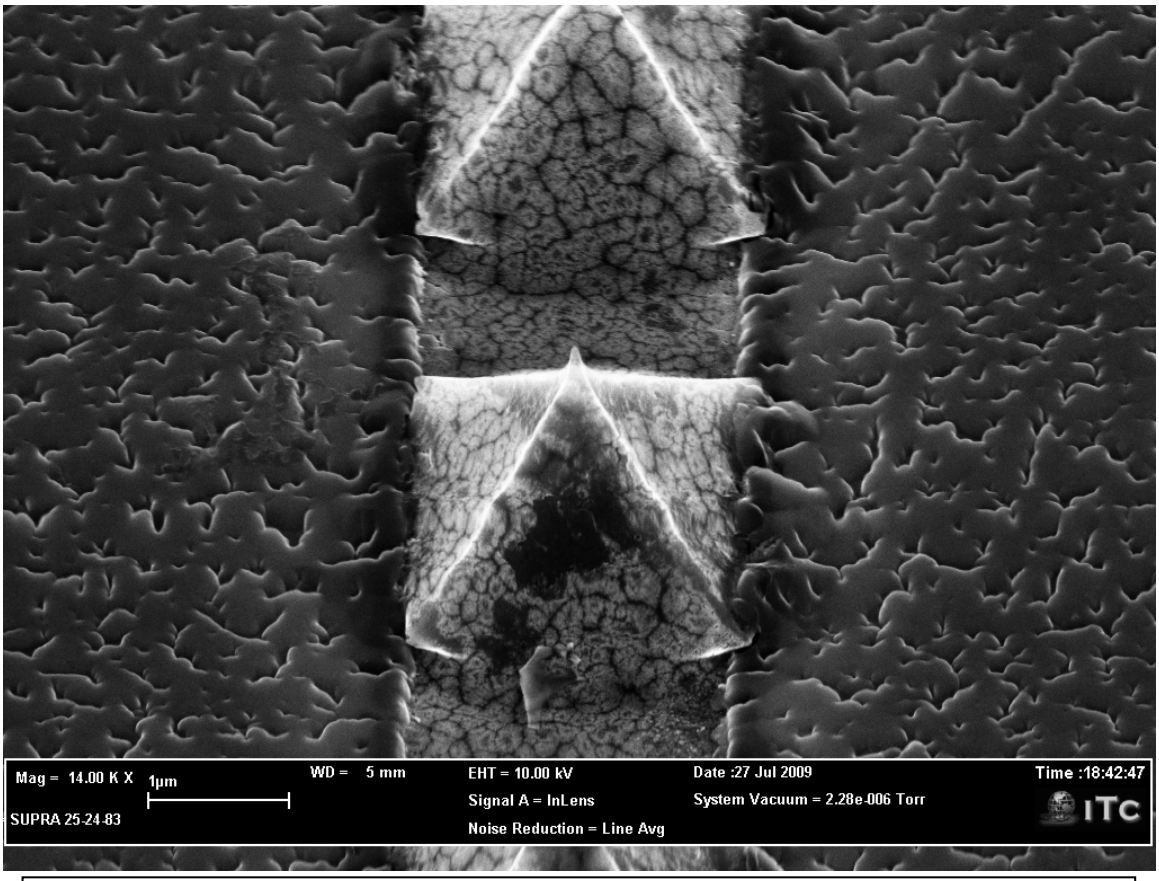


Figure 20: Diamond pyramidal tip and emission line between silicon nitride dielectric.

The final etch was another BOE dip to remove the thermal oxide layer directly above the diamond tips. BOE does etch silicon nitride, but at a slower rate than silicon dioxide, so care was taken not to overetch the samples in this final step. This final etch removed the silicon dioxide from the diamond tips and exposed the silicon nitride dielectric between the emission lines (Figure 18 (vii)). Figure 20 shows an SEM image of a released tip between two dielectric surfaces.

II.C Testing

II.C.I bgFEA testing

After the tips had been released, the sample was mounted in a 24 pin package using indium metal as a solder. The back-gate and cathode were wire bonded to different pins in the package, and it was prepared for testing. Field emission testing was performed at both Vanderbilt University and at ITC. One of the issues often associated with generating and testing FEAs is

achieving emission uniformity. Using a closely spaced fixed transparent anode coated with a phosphor, emission uniformity test were conducted with a setup as shown schematically in Figure 21.

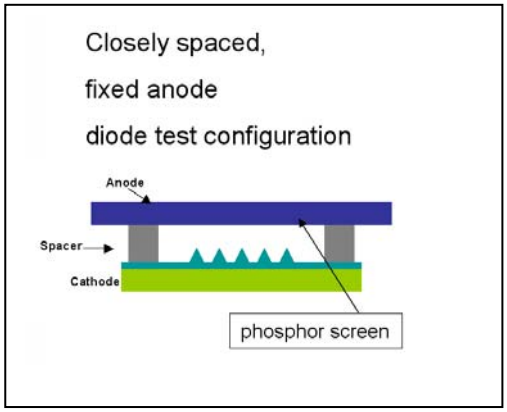
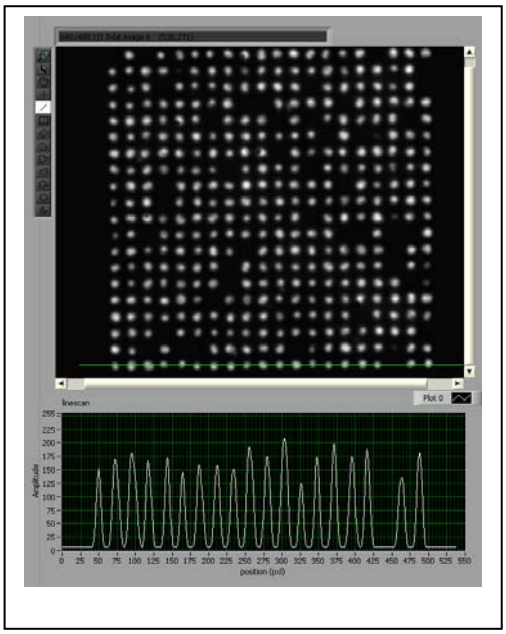


Figure 21: Emission test uniformity



Greater than 90% of the tips produce electron emission from a 20 x 20 array as highlighted by the emission from the phosphor coated anode. The test were conducted in pulse mode (100 µs) to avoid degradation of the phosphor.

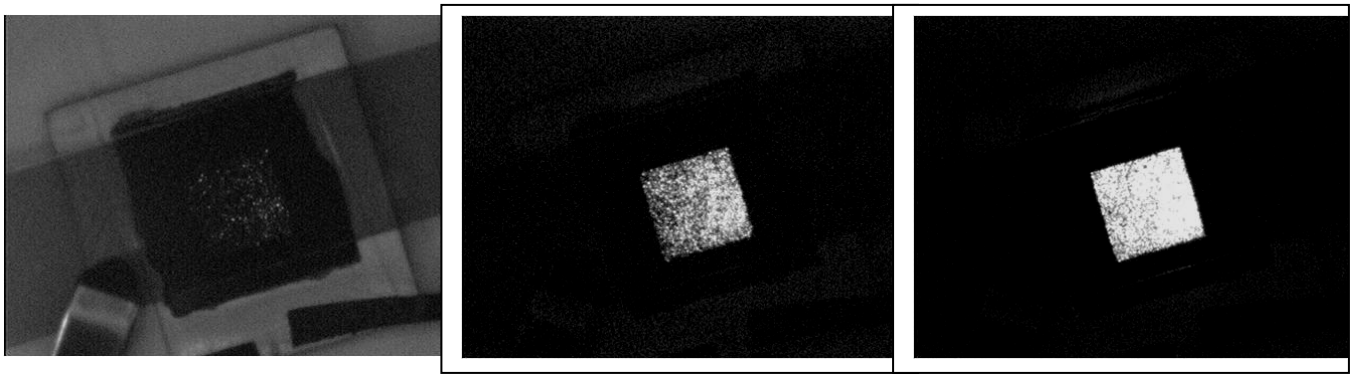


Figure 22: Field emission uniformity test as a function of voltage: 594 V (left), 770 V (middle) and 814 V (right).

Test in Figure 22 were performed in pulse mode (100 Hz, 1% duty, 100 µs). Very good emission uniformity was observed for the 224x224 array of tips with 10µm tip base & 20 µm pitch.

Figure 23: Pulsed field emission test in diode mode.

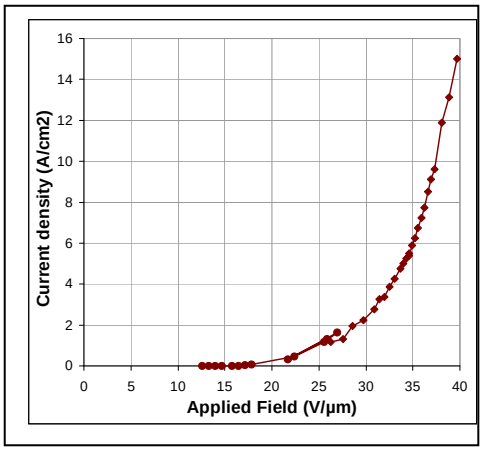
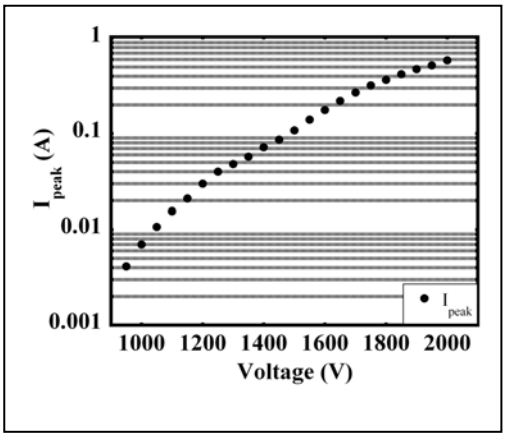


Figure 23 shows results for one of the best emission current density test as a function of applied field. The test was performed in diode mode and is composed of data taken in two different modes. The lower part of the curve was taken by adjusting the voltage on the anode; the top part of the curve was obtained by adjusting the position of the anode (approach curve method). That the two curves intersect and that the data was taken on two different days is an excellent indication of the reproducibility of the data. The maximum current density of 15 mA/cm^2 and maximum current of 15 mA is among the highest reported.

II.C.II Supporting Research



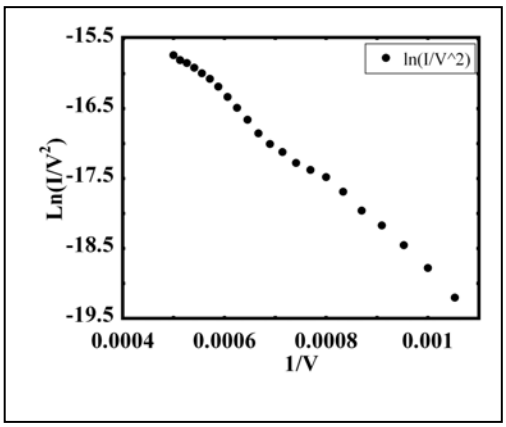


Figure 24: Emission current of 6oo mA from a non-HiFive cathode.

Figure 24 shows the emission current from a cathode from another program. An emission current of 600 mA was recorded equaling the highest recorded current from a cold cathode. The data was taken in pulse mode at 2 μs pulses. The tip base was 10μm and the current density was 6.1 mA/cm^2 showing that high current can be achieved with diamond-based cold cathodes.

II.D Conclusion

For high power, high frequency applications vacuum devices remain the only technology available. Most of these devices operate with thermionic electron sources, a technology that has drawbacks in terms of start-up time, power consumption and thermal management issues. While these devices have demonstrated high reliability, there has been a longstanding interest in field emission array devices as an alternative electron source that does not exhibit these drawbacks. Gated FEAs can provide instant turn on of a device, higher overall anode current, more efficient frequency modulation, space/weight savings, lower operating temperatures, and lower power consumption. However, there are still issues of reliability of the FEA devices and their output power (current density) needs to be increased, especially for microwave power amplifier applications. The integration of two of the leading cold cathode technologies, molded diamond tips and back-gate field-emission devices (bgFED) has been proposed in the current project to achieve these goals. Combining the two technologies provides the benefit of the stable high current density diamond tips and the arc-resistant long term performance of bgFEDs.

The back-gate design with the gate electrode positioned behind the array of FE tips minimizes the chance of arching. Further, the close proximity of the gate electrode to the emitter tips separated only by a thin intervening dielectric allows low gate voltage operation, <125 V, and as a consequence the energy of ions produced in the vicinity of the cathode is low and less likely to cause damage. The use of diamond as the emitter material provides a robust, low effective work function material that can be grown in silicon molds with a tip radius of ~ 5nm providing high field enhancement. Dopants introduced during the chemical vapor deposition of the diamond provide the electrically conductive tips and a separate more resistive layer, barrister, which serves as a means to achieve more uniform electron emission across an array.

Electrostatic modeling provided an optimum layout for the pitch between the diamond tips along the cathode lines as well as the pitch between cathodes lines. The field enhancement as a result of voltage applied to the back-gate was predicted to be between 10^2- 10^3 which is consistent with the previous experimental result of ~250. Diamond tip arrays laid out in the geometry suitable for the HiFive program have been fabricated and tested. A total emission current of 600 mA at

6.1A/cm^2 was produced matching the best know reported current from a single cathode. The best current density, 15 A/cm^2, at a high emission current 15 mA is arguable the highest reported for FE cathodes in light of achieving simultaneously both high current and current density. Both sets of data were obtained in pulse mode. The modeling predicts that the HiFive program goal of 750 A/cm^2 can be met with the present design and scaling the tip base as a next step to increase the tip density and enhance the electrostatic field at the tip will more than double the current and current density providing cathodes that exceed the requirements of the HiFive program without any additional enhancements. Process studies were conducted to achieve predictable yield of diamond tips with small radius. A barrister layer was developed as a base layer for the diamond tip array as a means to achieve more uniform electron emission across an array of tips. A process was developed to integrate the back-gate electrode with the diamond tip array taking into consideration a variety of issues such as the deposition process, adhesion, etch selectivity, and coefficient of thermal expansion. The process is poised upon review to produce cathodes for the HiFive program and other applications.

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